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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/717,506	11/21/2003	Fumihito Ohta	245696US2	7630

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EXAMINER	
TABONE JR, JOHN J	
ART UNIT	**PAPER NUMBER**
2138	

DATE MAILED: 04/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/717,506	OHTA, FUMIHITO	
	Examiner	Art Unit	
	John J. Tabone, Jr.	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 November 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11212003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-15 have been examined.

Drawings

2. The drawings are objected to because descriptive labels other than numerical are needed for figure 1. See 37 CFR 1.84(o). The boxes should be made larger, if need be, to accommodate appropriate labels. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance. Further, the figures that illustrate the matrix of rows and columns, namely Figures 3, 4A, 5A, 6, 8-10 and 12-14, should be amended to show the column and row numbers referred to in the specification for those figures. For example, in the discussion of Fig. 3 on page 7, the Applicant refers to certain failed bits in various rows and columns, such as first row, tenth row, twentieth row, etc. These rows and columns should be numbered to correspond to the specification as to better facilitate correlating the Figure to the discussion in the specification. Figures 3, 4A, 5A, 6, 8-10 and 12-14, should be amended in response to this Office Action.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure

number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claims 2-15 are objected to because the step designations h-z cannot be executed in secession as listed. Claims 2, 4, 7, 9, 11 and 14 are on one side of the claim tree and claims 3, 5, 8, 10, 12 and 15 on the other. The Examiner assumes the Applicant intended to execute these steps in secession, indicated from claim 13. The step designators in the claims should be corrected as to indicate the proper order of the claim method according to the claims dependencies.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 4 and 5 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claims 3 and 4:

These claims recite converting each column or row to a failure bit (digital 1) of a normal bit (digital 0) with respect to "the predetermined number of failure bits" (also see 35 U.S.C. 112, second paragraph rejection below). The specification discloses on page 7, lines 17-25, the converting method is with respect to "the corresponding threshold value" not "the predetermined number of failure bits". Therefore, these claims fail to comply with the enablement requirement and will not be further examined in the merits.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1:

This claim recites the limitation "finding a first threshold value from an average value of said number of failure bits with respect to each row in step (c) and with respect to each row in step (d). The Examiner does not know if "an average value" is the same or different than the "average value" calculated in steps (e) and (f). This renders the claim vague and indefinite. The Examiner suggests changing this limitation to "finding a first threshold value from one-half of an average number of failure bits..." as disclosed in the specification on page 7.

Claims 3 and 4:

These claims recite the limitation "the predetermined number of failure bits" and "said predetermined number". There is insufficient antecedent basis for this limitation in the claims.

Claim 6:

This claim recites the limitation "said failure bit map". There is insufficient antecedent basis for this limitation in the claim. This should read, "said fail bit map".

Claim 13:

a). The claim limitation "a predetermined value" renders the claim indefinite because it is not clear whether this is the same or a different "predetermined value" from the "predetermined factor" recited in claim 1, in which claim 13 depends. Correction and clarification is required.

b.) This claim recites the limitation "said steps (a) through (x) are omitted". There is insufficient antecedent basis for steps (h) through (x) in the claim since claim 1, from which claim 13 depends, only has steps (a) through (g).

As a result of the problems with this claim it will not be further examined in the merits.

Claims 2-15:

These claims are also rejected because they depend on claim 1 and have the same problems of indefiniteness.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3, 7-12, 14 and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Rathei (US-6553521).

Claim 1:

Rathei teaches a failure analysis method of a semiconductor device. Rathei also teaches in a fail bit map obtained from a semiconductor device including a plurality of memory cells arranged in a matrix (Col. 1, ll. 21-22). Rathei further teaches counting the

number of failure bits with respect to each row of a region classified as a block failure and counting the number of failure bits with respect to each column of said region (word and bit lines) (Col. 4, ll. 40-42). Rathei teaches finding a first threshold value from an average value of said number of failure bits with respect to each row (Col. 4, ll. 61-67), to compare said number of failure bits with respect to each row and said first threshold value (Col. 3, ll. 6-15, col. 5, ll. 16-29) and finding a second threshold value from an average value of said number of failure bits with respect to each column (Col. 4, ll. 61-67), to compare said number of failure bits with respect to each column and said second threshold value (Col. 3, ll. 6-15, col. 5, ll. 16-29). Rathei also teaches calculating an average value of a result of comparison with respect to each row as an average value of rows and calculating an average value of a result of comparison with respect to each column as an average value of columns. (Col. 3, ll. 27-31. Rathei further teaches determining that said semiconductor device contains a block failure in a column direction, a block failure in a row direction, or a random block failure, said block failure in a column direction satisfying a condition that said average value of rows is greater than a value obtained by multiplying said average value of columns by a predetermined factor, said block failure in a row direction satisfying a condition that said average value of columns is greater than a value obtained by multiplying said average value of rows by said predetermined factor, said random block failure satisfying conditions that said average value of rows is not more than a value obtained by multiplying said average value of columns by said predetermined factor, and said average value of columns is

not more than a value obtained by multiplying said average value of rows by said predetermined factor. (Col. 5, ll. 32-63). (Also, see col. 1, l. 41 to col. 6, l. 16).

Claim 2:

Rathei teaches dividing said fail bit map in a column direction, classified as said block failure in a column direction, into equal sections with respect to the certain number of columns, counting the respective numbers of failure bits existing in the same-numbered columns in all of said sections, to calculate the number of failure bits in each column of a group as an aggregate of said sections of columns and finding a third threshold value from a maximum value of the number of failure bits in each column of said group, and comparing said third threshold value and the number of failure bits in each column, to extract a column having the number of failure bits greater than said third threshold value. (Col. 1, l. 41 to col. 6, l. 16).

Claim 3:

Rathei teaches dividing said fail bit map in a row direction, classified as said block failure in a row direction, into equal sections with respect to the certain number of rows, counting the respective numbers of failure bits existing in the same-numbered rows in all of said sections, to calculate the number of failure bits in each row of a group as an aggregate of said sections of rows and finding a fourth threshold value from a maximum value of the number of failure bits in each row of said group, and comparing said fourth threshold value and the number of failure bits in each row, to extract a row having the number of failure bits greater than said fourth threshold value. (Col. 1, l. 41 to col. 6, l. 16).

Claim 6:

Rathei teaches previously defining an extent of said failure bit map as a target for the failure analysis method. (Col. 1, l. 41 to col. 6, l. 16).

Claim 7:

Rathei teaches on the basis of a result of extraction in said step (j), calculating periodicity in frequency of occurrence of failure bits in a column direction. (Col. 1, l. 41 to col. 6, l. 16).

Claim 8:

Rathei teaches on the basis of a result of extraction in said step (m), calculating periodicity in frequency of occurrence of failure bits in a row direction. (Col. 1, l. 41 to col. 6, l. 16).

Claim 9:

Rathei teaches removing failure bits having said periodicity in a column direction from said fail bit map. (Col. 1, l. 41 to col. 6, l. 16).

Claim 10:

Rathei teaches removing failure bits having said periodicity in a row direction from said fail bit map. (Col. 1, l. 41 to col. 6, l. 16).

Claim 11:

Rathei teaches on the basis of remaining failure bits, performing data complement on said fail bit map from which failure bits having said periodicity in a column direction have been removed. (Col. 1, l. 41 to col. 6, l. 16).

Claim 12:

Rathei teaches on the basis of remaining failure bits, performing data complement on said fail bit map from which failure bits having said periodicity in a row direction have been removed. (Col. 1, l. 41 to col. 6, l. 16).

Claim 14:

Rathei teaches classifying said block failure having said periodicity in a column direction on the basis of information indicative of a proportion of failure bits and a distribution of failure bits in said block failure. (Col. 1, l. 41 to col. 6, l. 16).

Claim 15:

Rathei teaches classifying said block failure having said periodicity in a row direction on the basis of information indicative of a proportion of failure bits and a distribution of failure bits in said block failure. (Col. 1, l. 41 to col. 6, l. 16).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ishihara et al. (US006404911)

Ishihara a failure analysis system which substantially teaches various aspects of the claimed invention namely, failure bit maps, block error in both columns and rows as well as several compression techniques to compress the failure data. (Claims 1-15).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (571) 272-3827. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John J. Tabone, Jr. 4/21/06
Examiner
Art Unit 2138

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